

Notice of References Cited

Application/Control No.

10/730,120

Applicant(s)/Patent Under
Reexamination
SHIBATA, KOHSAKU

Examiner

Kandasamy Thangavelu

Art Unit

2123

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,051,309	05-2006	Crosetto, Dario B.	716/10
*	B	US-6,871,298	03-2005	Cavanaugh et al.	714/33
*	C	US-6,397,324	05-2002	Barry et al.	712/225
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sami et al., "An instruction level energy model for embedded VLIW architectures" IEEE, September 2002.
	V	Jee et al., "Performance evaluation for a compressed VLIW processor", ACM, March 2002.
	W	Jouppi et al., "Available instruction level parallelism for superscalar and superpipelined machines", ACM 1989
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.